	Doc No	SDSC-PSE-A	NJIETH
Prepared King.	Product Specifications	EXTERN	AL ISSUE
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Structure	Silicon Monolithic Bipolar IC
Appearance	SIL-12 Pin Plastic Package (Power Type with Fin attached)
Application	Hi-Fi and Car Stereo
Function	BTL 23W Audio Power Amplifier

A	Absolute Maximum Ratings				
No.	Item	Symbol	Ratings	Unit	Note
1	Storage Temperature	Tstg	-55 ~ +150	°C	1
2	Operating Ambient Temperature	Topr	-30 ~ +75	°C	1
3	Supply Voltage	Vcc	26	V	
4	Supply Current	Icc	4.0	А	
5	Power Dissipation	PD	62.5	W	
6	Surge Voltage	V _{surge}	50	V	

Note: 1) The temperature of all items shall be Ta=25°C except storage temperature and operating ambient temperature.



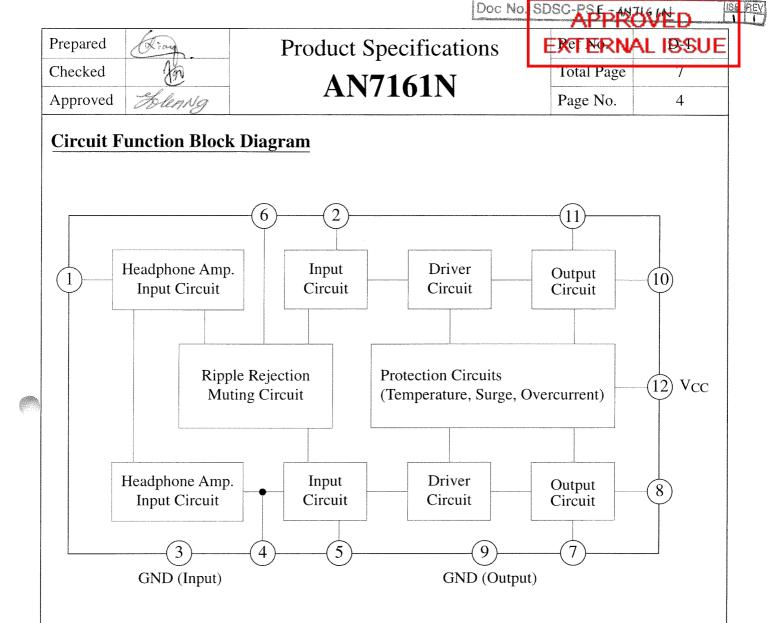
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В	Eleo	ctrical Characte	ristics (Unle	ss otherwise specified, the a	ambient	tempe	rature i	s 25°C ±	2°C)
.	T			Test			Limits	5	T T • .	
No	Item		Symbol	Cir- cuit		min	typ	max	Unit	Note
1	Quie Curr	escent Circuit ent	I _{CQ}	1	V _{CC} =15V, V _{in} =0V	-	45	75	mA	
	Pow	er Amplifier (V _{CC}	=15V, RL	,=4Ω	e, freq.=1kHz)					
2	Outŗ	out Noise Voltage	V _N	1	$\begin{array}{l} f=15Hz \sim 30 kHz, \\ 12 dB/oct, R_g=10 k\Omega \end{array}$	_	0.6	1.0	mV	
3	Volta	age Gain	Gv	1	V _{in} =5mV	48.5	50.5	52.5	dB	
4		l Harmonic ortion	THD	1	V _{in} =5mV	-	0.15	0.5	%	
5	Max Outp	imum Power out	Po	1	THD=10%	20	23	-	W	
6	Outr Volta	out Offset age	V _{OS}	1	Rg=0Ω	-	-	150	mV	
	Head	lphone Amplifier (V _{CC} =15V	/, R _L	=33 Ω , freq.=1kHz)					
7	Outp	out Noise Voltage	V _{N-H}	1	f=15Hz ~ 30kHz, 12dB/oct, R_g =10k Ω	-	0.1	0.7	mV	
8	Volta	age Gain	G _{V-H}	1	V _{in} =10mV Power Amplifier mute	17.5	19.5	21.5	dB	
9	Max Powe	imum Output er	P _{O-H}	1	THD=1% Power Amplifier mute	10	-	-	mW	

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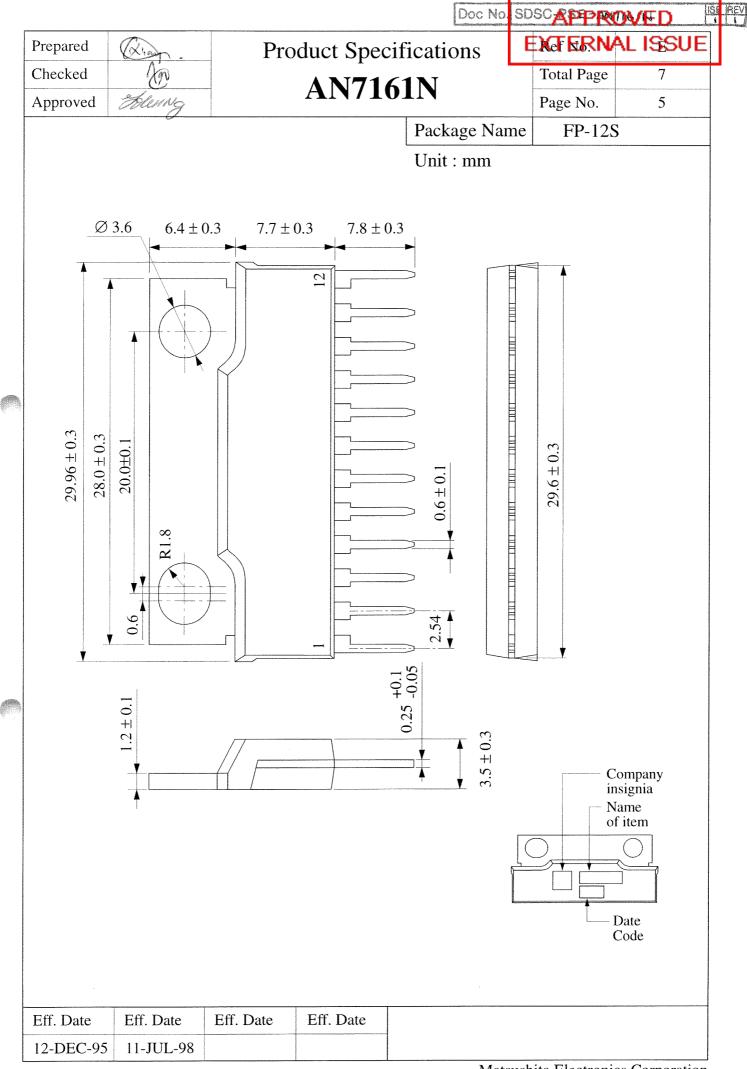
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	$\begin{array}{c} 3.5 \vee 50 \\ \hline 100 \mu 2 \\ \hline 33 \mu \\ \hline 12 \\ \hline 777 \\ \hline 777 \\ \hline 12 \\ \hline 12 \\ \hline 777 \\ \hline 12 \\$		AN7161N	5_9 47µ 0.01µ 7/7 7/7		/// /// /// /// /// /// /// ///		1μ 	
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Pin Descriptions

Pin No.	Description	Pin No.	Description
1	Output (Headphone)	7	Bootstrap Channel 1
2	Negative Feedback Channel 2	8	Output Channel 1
3	GND (Input)	9	GND (Output)
4	Input	10	Output Channel 2
5	Negative Feedback Channel 1	11	Bootstrap Channel 2
6	Ripple Filter	12	Vcc

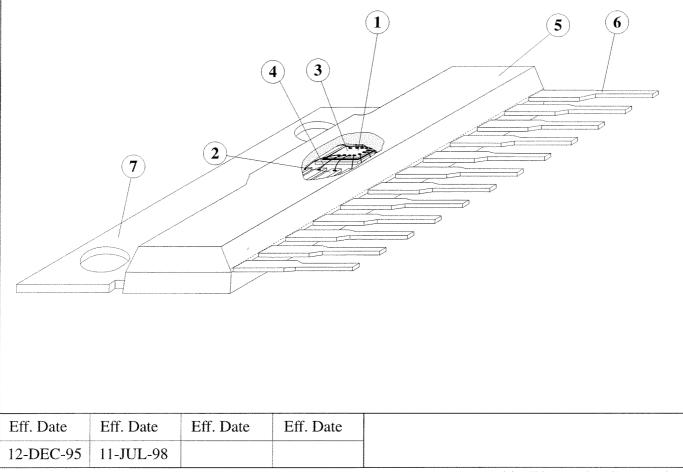
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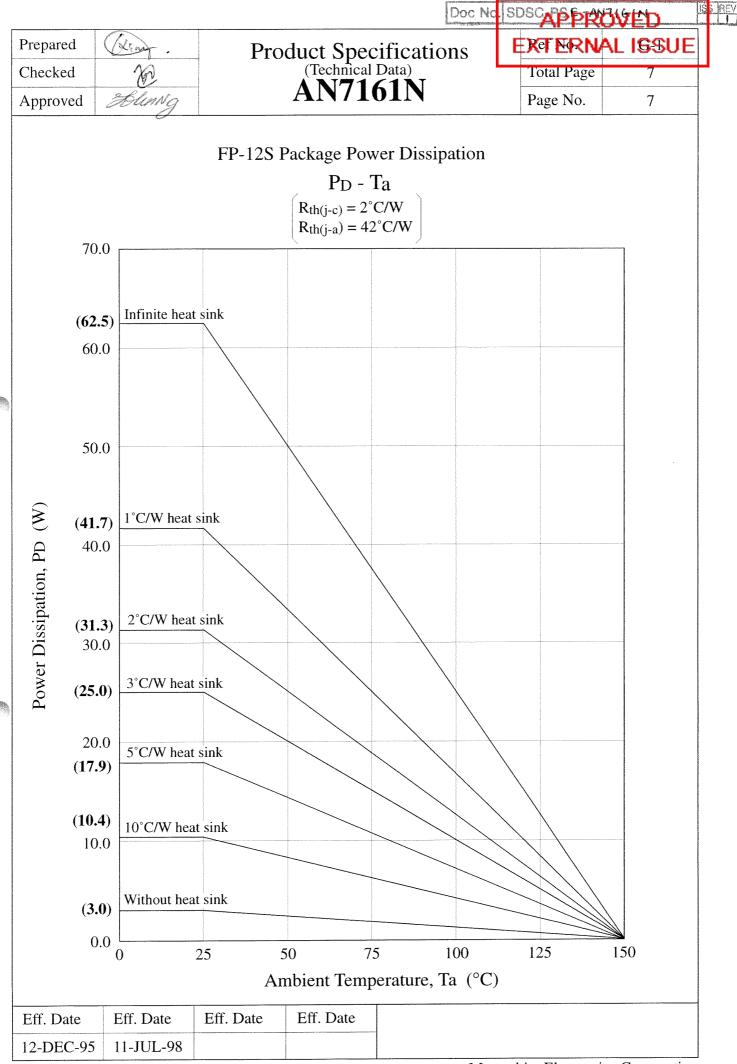


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(Structu	re Descriptio	n)				
Chip surfac	ce passivation	SiN,	PSG,	Othe	rs ()	1
Lead frame	e material	Fe group,	Cu group,	Othe	rs ()	2,6
Inner lead	surface process	Ag plating,	Au plating,	Othe	rs ()	2
Outer lead	surface process	Solder plating,	Solder dip,	Othe	rs ()	6
Chip moun	ting method	Ag paste,	Au-Si alloy, Solder,	Othe	rs ()	3
Wire bondi	ng method	Thermalsonic bo	onding,	Othe	rs ()	4
Wire mater	ial, Diameter	(Au,	Diameter <u>50</u> µm	Other	rs ()	4
Mold mate	rial	Epoxy,		Other	rs ()	5
Molding m	ethod	Transfer mold,	Multiplunger mold,	Other	rs ()	5
Fin materia	1	Cu Group		Other	/ ``	(7)

Package FP-12S

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